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Dr. Shounak Chakraborty

Current Position

I am a **Post Doctoral Fellow (through ERCIM Fellowship)** at the **Dept. of Computer Science, NTNU, Trondheim, Norway** since January 1, 2019, working with **Prof. Magnus Själander**. Primarily, my broad research area is Computer Architecture, where during my PhD I worked towards improving **Energy & Thermal Efficiency** of Chip Multi-Processors and in my current post-doctoral work I am mostly focusing on improving thermal efficiency of heterogeneous multi-cores.

Education

Doctor of Philosophy (Computer Sc. & Engineering) December 2011 – February 2018
Indian Institute of Technology Guwahati
- Thesis Supervisor: Prof. Hemangee Kalpesh Kapoor
- Title of Thesis: Energy and Thermal Management of CMPs by Dynamic Cache Reconfiguration

Master of Engineering(Computer Sc. & Engineering) August 2009 – July 2011
College of Engineering Guindy, Anna University Chennai, India
- CPI: 7.85/10

Bachelor of Technology(Computer Sc. & Engineering) August 2005 – June 2009
MCKV Institute of Engineering, Liluah, Howrah, India (MAKAUT, formerly known as WBUT)
- CGPA: 8.01/10

Higher Secondary Examinations July 2003 – June 2005
Anandamath Vidyapith (WBCHSE), West Bengal, India
- Marks Percentage: 77.4%

Secondary Examination June 2003
Bhogpur K.M. High School (WBBSE), West Bengal, India
- Marks Percentage: 76.6%

Research Interests

My research interest currently focuses on the following areas of Modern Computer Architecture-
- Power & Thermal Efficiency
- Memory Technologies
- Caches and Cores
- SoC design

I am also interested to expand the boundaries of my work between Application, Operating System, Compilers and Hardware.

Selected Publications

Journal

Published/Accepted

- **S. Chakraborty**, and H. K. Kapoor, "Exploring the Role of Large Centralised Caches in Thermal Efficient Chip Design." *ACM Trans. Des. Autom. Electron. Syst. **[TODAES]***, Vol. 24, Issue 5, Article 52, June 2019, 28 pages.
- **S. Chakraborty**, and H. K. Kapoor, "Analysing the Role of Last Level Caches in Controlling Chip Temperature", *IEEE Transactions on Sustainable Computing **[TSUSC]***, Vol. 3, No. 4, Oct.-Dec. 2018, Pages 289-305.
- **S. Chakraborty**, and H. K. Kapoor, "Performance linked Dynamic Cache Tuning: A Static Energy Reduction Approach in Tiled CMPs", *Journal of Microprocessors and Microsystems (Elsevier) **[MICPRO]***, Volume 52, July 2017, Pages 221-235.

Conference

- A. A. Kulkarni, **S. Chakraborty**, S. P. Mahajan, H. K. Kapoor, "Utility Aware Snoozy Caches for Energy Efficient Chip Multi-Processors"-*GLSVLSI 2018*, Chicago, Illinois, USA.

- **S. Chakraborty**, and H. K. Kapoor, "Towards Controlling Chip Temperature by Dynamic Cache Reconfiguration in Multiprocessors"-*30th International Conference on VLSI Design (VLSID)*, 2017, pp. 75-80, Hyderabad, India.
- **S. Chakraborty**, and H. K. Kapoor, "Static Energy Reduction by Performance Linked Dynamic Cache Resizing"-*IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2016, pp. 1-6, Tallinn, Estonia.
- **S. Chakraborty**, S. Das and H. K. Kapoor, "Static Energy Efficient Cache Reconfiguration for Dynamic NUCA in Tiled CMPs"-*Proceedings of the 31st Annual ACM Symposium on Applied Computing (SAC '16)*, 2016, pp. 1739–1744, Pisa, Italy.
- H. K. Kapoor, S. Das and **S. Chakraborty**, "Static energy reduction by performance linked cache capacity management in Tiled CMPs"-*Proceedings of the 30th Annual ACM Symposium on Applied Computing (SAC '15)*, 2015, pp. 1913–1918, Salamanca, Spain.
- **S. Chakraborty**, S. Das and H. K. Kapoor, "Performance constrained static energy reduction using way-sharing target-banks", *IEEE International Parallel and Distributed Processing Symposium Workshop (IPDPSW '15)*, 2015, pp. 444-453, Hyderabad, India.
- **S. Chakraborty**, S. Das and H. K. Kapoor, "Power Aware Cache Miss Reduction by Energy Efficient Victim Retention"- *19th International Symposium on VLSI Design and Test (VDAT '15)*, 2015, pp. 1-6, Ahmedabad, India.
- N. K. Meena, H. K. Kapoor, **S. Chakraborty**, "A New Recursive Partitioning Multicast Routing Algorithm for 3D Network-on-Chip". *18th International Symposium on VLSI Design and Test (VDAT '14)*, 2014, pp. 1-6, Coimbatore, India.

PhD Forum (Poster Presentation)

- VLSI Design 2017, VLSI-SoC 2016

Skill Set

- **Programming Languages:** JAVA, C++, C, Python
- **Hardware Simulators:** CACTI, Simics, GEMS, HotSpot, Multi2Sim, McPAT, NVSim, DESTINY, Gem5
- **Mathematical Tools:** MATLAB, PRISM, MAPLE

Short Abstract of PhD Thesis

Title: Energy and Thermal Management of CMPs by Dynamic Cache Reconfiguration

To commensurate the high data demand in recent CMPs (Chip Multi-Processors), equipped with a number of cores, large on-chip LLCs (Last Level Caches) are attached. By studying a plethora of prior works, it has been concluded that, LLCs play a vital role in maintaining system performance. But large sized LLCs are accounted for their significant leakage energy consumption, which has a circular dependency on effective temperature of the chip. In addition with curtailing circuit's reliability, this increased chip temperature has enough potential to damage the on-chip circuitry permanently.

In our work, we initially proposed a set of performance constrained Dynamic Cache Resizing techniques to reduce leakage in LLCs. The resizing is done by turning off/on some cache banks which can be implemented by power gating at circuit level. The cache resizing decision is triggered based upon the dynamic change in system performance. We get 65% savings in leakage energy consumption. Apart from bank level granularity, we have also proposed cache resizing at way-level granularity, where performance degradation is handled by incorporating DAM (Dynamic Associativity Management). In this policy, we have 70% improvement in leakage energy. However, from thermal efficiency perspective, these turned-off cache portions are utilised as on-chip thermal buffer to reduce effective chip temperature, especially in CMPs having larger LLCs. The gained energy and thermal benefits are studied (i) for a Tiled CMP architecture and (ii) for a CMP having centralised LLC. For Tiled CMP, we get a reduction of around 4°C for average chip temperature, which is closer to 6°C in CMPs having centralised LLC.

Work Experience

- Designation : Post Doctoral Fellow,
  Current Research Focus: Heterogeneous CMPs, Energy & Thermal Efficiency.
  Organization: Norwegian University of Science & Technology (NTNU), Trondheim, Norway.
  Duration: January 1, 2019 to *till date*.

- Designation : Assistant Professor,
  Organization: Indian Institute of Information Technology Guwahati, Guwahati, Assam, India.
  Duration: July, 2018 to December, 2018.
  Courses Taught: Compilers (UG), Compiler Lab (UG)

- Designation : Assistant Professor,
  Organization: Future Institute of Engineering & Management, Kolkata, West Bengal, India.
  Duration: July, 2011 to December, 2011.
  Courses Taught: Compiler Design (UG), DBMS (UG)

List of Courses Assisted as TA (During PhD)

- **UG Courses:** Computer Architecture & Organisation (Once), Introduction to Computing (Twice), Digital Design (Twice), Programming Lab (Once), Microprocessor Lab. (Once)
- **PG Courses:** Advanced Computer Architecture (Twice), Parallel Computer Architecture (Once).

Invited Talk/Seminar

- Delivered talk on "Energy and Thermal Management of CMPs" at **Dept. of CSE, IIT Delhi, India** on May 8, 2018.
- "TECTONIC: Towards Employing Compilers for Thermal Management and Optimal Data Placement in Hybrid Cache" at **ARM Research Summit 2019, Texas, USA** during Sept. 15 to 18, 2019.

Awards

- Received **Marie Skłodowska-Curie Actions-Individual Fellowship (MSCA-IF)** from Euroepan Commission for **Post Doctoral Research at NTNU, Trondheim, Norway**

  Project Title: TECTONIC (Towards Employing Compilers for Thermal Management and Optimal Data Placement in Hybrid Cache)

  Duration: 24 months (January 1, 2021 to December 31, 2022)

  Amount: EUR 214,158.72
- Selected in "**ERCIM Alain Bensoussan Fellowship Programme**" (supported by the FP7 Marie Curie Actions) of the European Commission for doing **Post Doctoral Research at NTNU, Trondheim, Norway** (From January 1, 2019 to December 31, 2020).
- Received travel grant for attending **VLSI Design 2017** at Hyderabad, India.
- Received travel grant from **Student Travel Award Program of ACM-SIG** for attending **ACM SAC 2016** at Pisa, Italy.
- Received travel grant from **IFIP/IEEE** for attending **VLSI SoC 2016** at Tallinn, Estonia.
- Received student travel grant for attending **IPDPS 2015** at Hyderabad, India.
- Received **MHRD Scholarship, Govt. of India** for 5 years during PhD at IIT Guwahati, India.
- Received **MHRD Stipend, Govt. of India** for 2 years Masters study at College of Engineering Guindy, Anna University Chennai, India by qualifying **GATE 2009 in Computer Science, with All India Rank 874 out of 43170 candidates**.

Declaration

I do hereby declare that the particulars of information and facts stated herein above are true, correct and complete to the best of my knowledge and belief.

Date: 10-Mar-2020
Place: Trondheim

Signature
(SHOUNAK CHAKRABORTY)